

FIG. 1

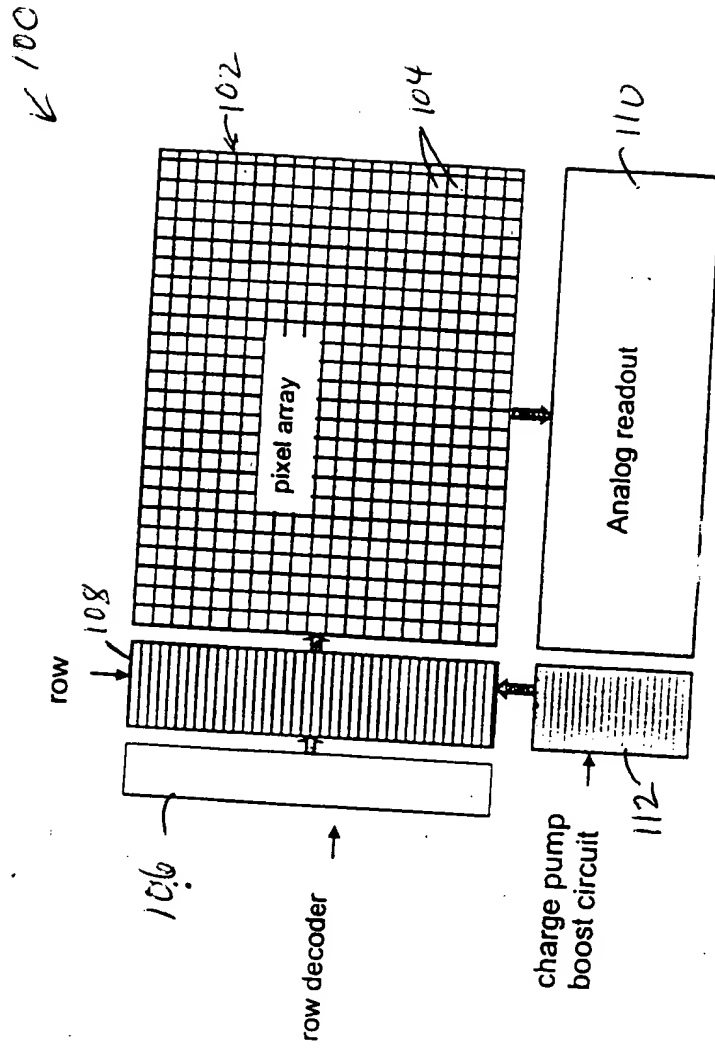


FIG. 1

1. The circuit is a schematic diagram of a memory array, specifically a 1T1R1C1 (1 Transistor, 1 Row, 1 Column) array. It shows the internal structure of a memory cell and the associated control logic.

200V

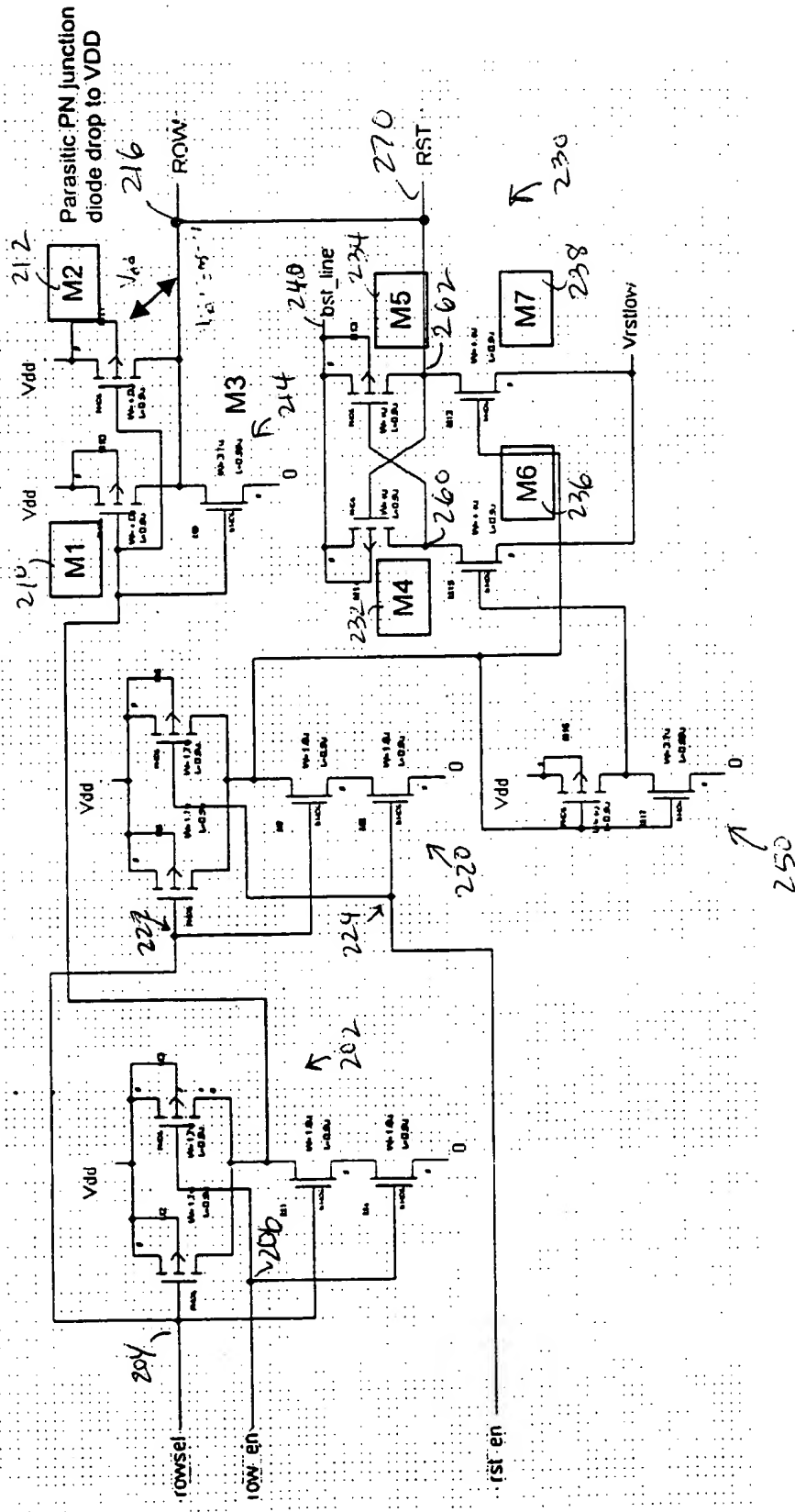


FIG. 2

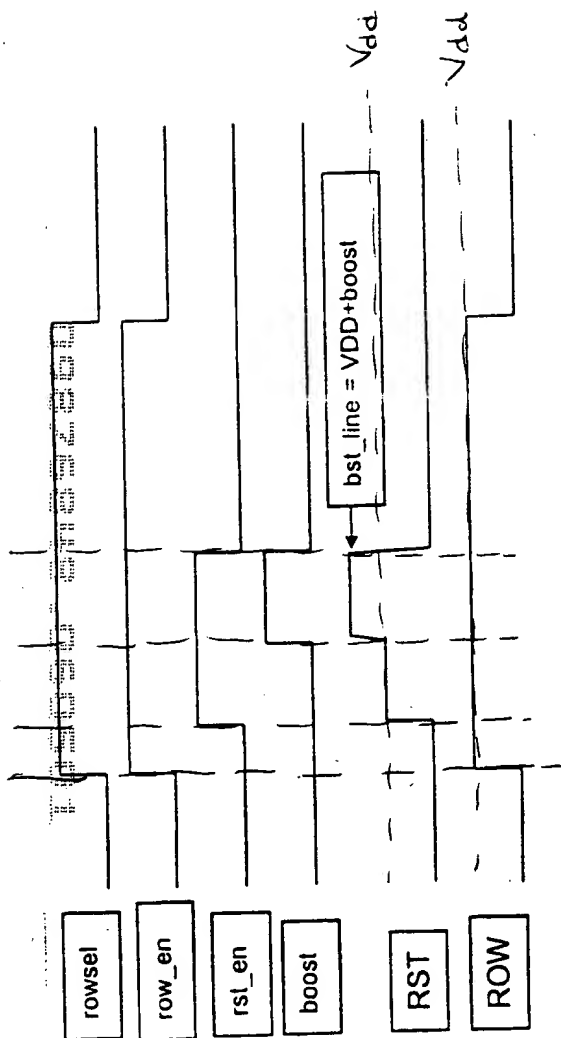


FIG. 3

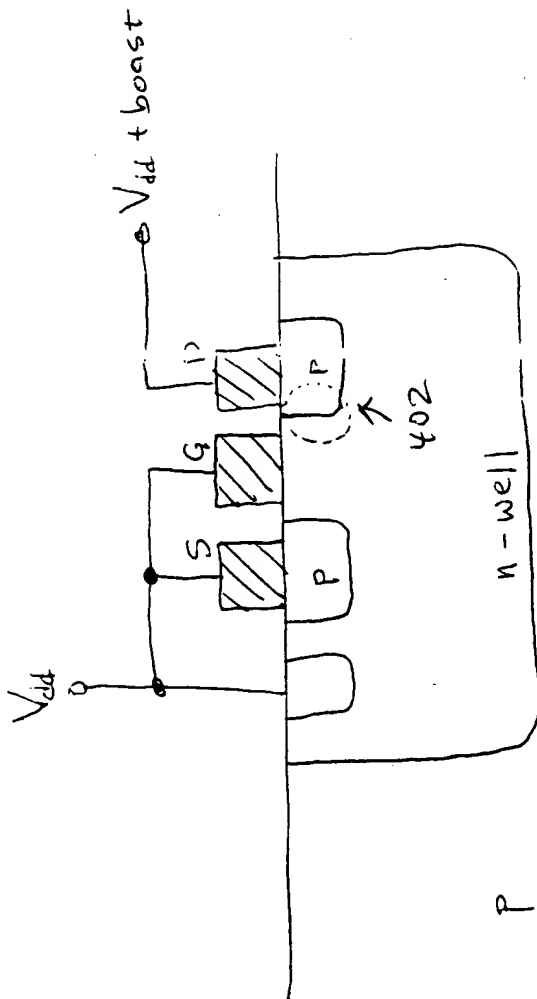


FIG. 4

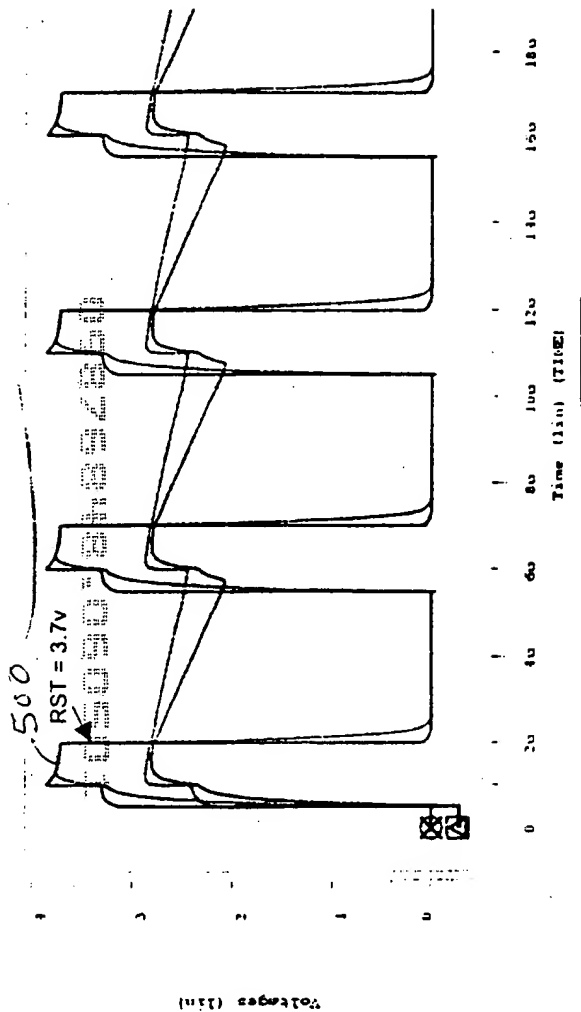


FIG. 5

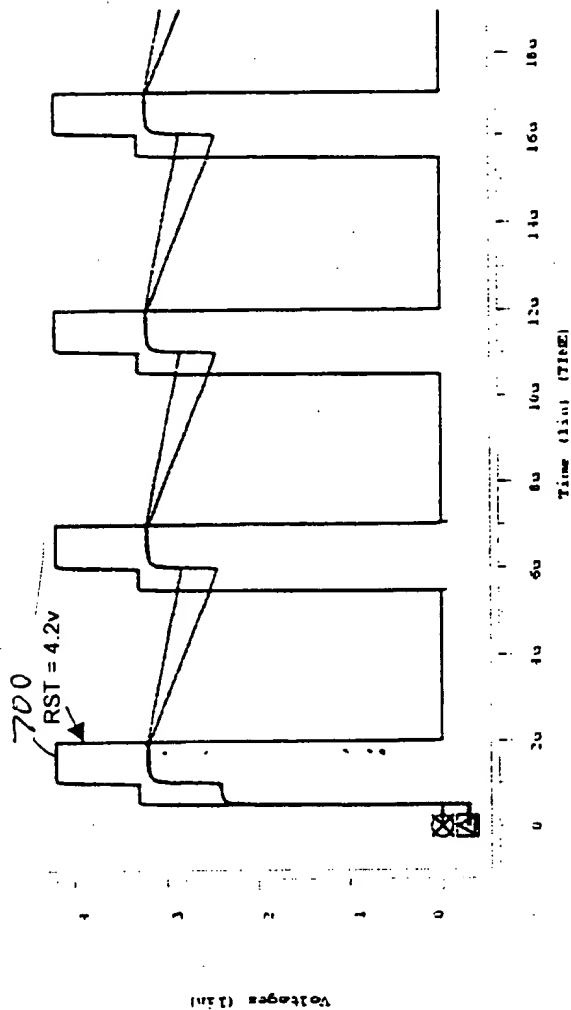


FIG. 7

FIG. 6

600

Boost the Nwell to remove the parasitic PN junction diode drop.

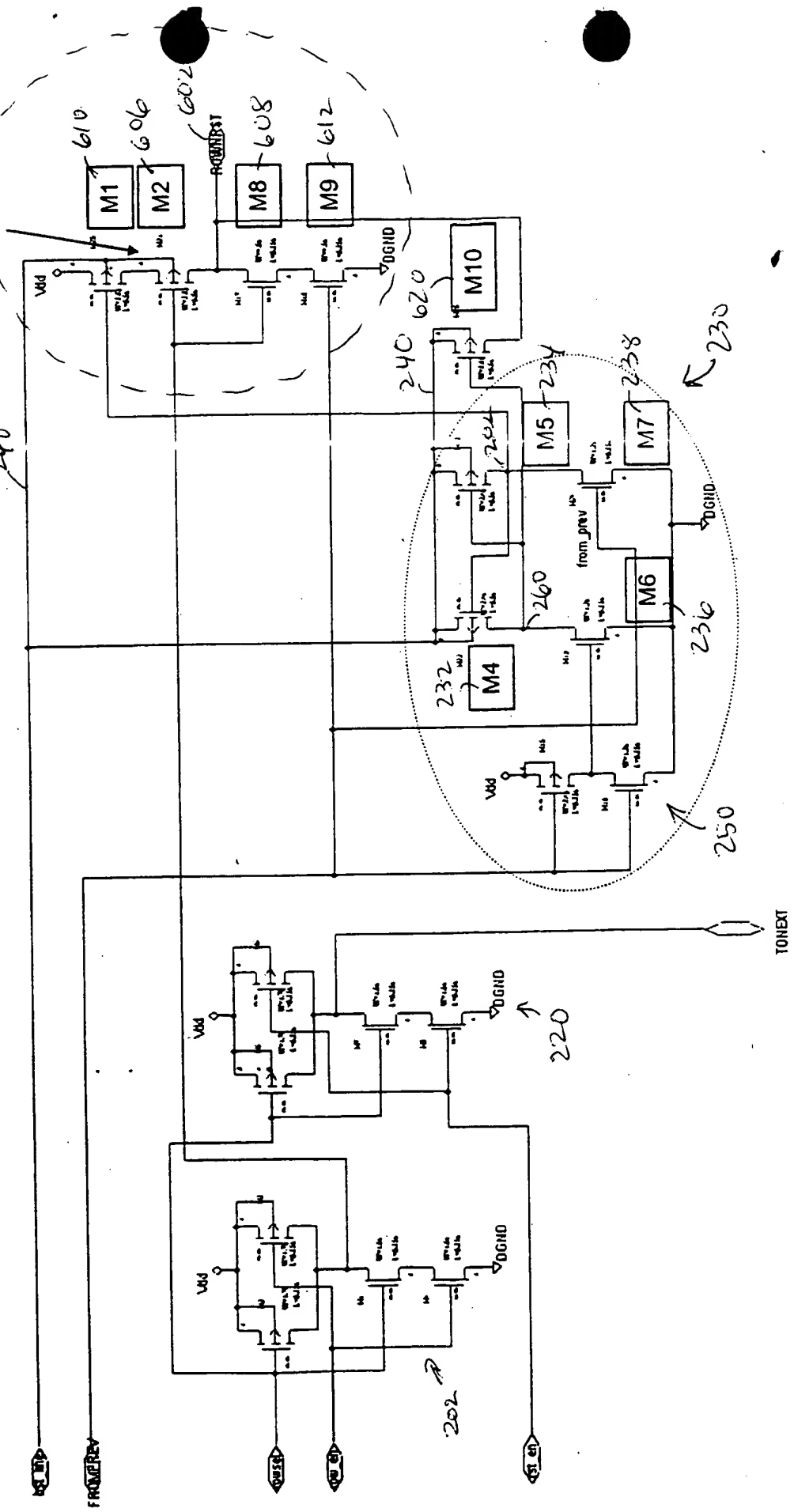


FIG. 6